ABSTRACT

A test circuit for integrated circuit devices is disclosed, which can shorten the test time, and can reduce the length of the test pattern and the number of external terminals. The test circuit is provided between first and second target circuits, and comprises a section for selecting one of a first output signal from the first target circuit, a second output signal from the second target circuit, and a test signal indicating a test pattern input via a test pattern input terminal, according to first and second test mode signals supplied from an external device; a section for temporarily storing the signal selected by the first section as a data signal; a section for selecting one of the temporarily stored data signal or the second output signal according to the second test mode signal, and providing the selected signal to the first target circuit; and a section for selecting one of the temporarily stored data signal or the first output signal according to a third test mode signal supplied from an external device, and providing the selected signal to the second target circuit. The temporarily stored data signal is also output as a test result via a test pattern output terminal.